Front End Electronics for the STAR TPC

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1998 marked the successful conclusion of STAR TPC Front End Electronics design, smooth production of the virtually all of the hardware, and a solid start on installation.

The TPC FEE receives signals from the 136,600 pads on the TPC, amplifies them, shapes them, and digitizes them with a 512 time sample, 6/12 MHz, 10 bit waveform digitization system[1]. This digitization is done on 4,400 FEE cards which plug into the TPC pad planes. Each FEE card contains two 16 channel preamplifier/shaper chips, followed by two 16 channel switched capacitor array/ADC chips. Each channel includes a 512 time bucket switched capacitor array and a 12 bit ADC. These boards were populated at Max Planck Institute, Munich (MPI), and tested and mechanically assembled at LBNL. About 90% of the cards were installed in in the STAR TPC in 1998.

Up to 36 FEE cards are read out by a single readout board, which multiplexes the data and sends it to the data acquisition system over 1.2 Gbit/sec fiber optic links. The design of this board was finalized in 1998, and the 160 (including spares) readout boards produced.

One crucial component of the FEE system is the switched capacitor array acquisition clock. The system uses a single clock, which is generated on a clock and trigger distribution board, and distributed differentially to all 144 readout boards. Each time the TPC triggers, this clock generates 512 pulses. There are stringent requirements on drift; the clock must be stable to 50 ppm to avoid impacting hit reconstruction. At the same time, it must produce a range of frequencies to accommodate a range of TPC drift velocities. It must be able to start phase synchronously on any given beam crossing when a STAR trigger occurs. The current design is is based on an analog delay line, where the delay time is controlled by an adjustable voltage. The delay line is temperature controlled, and meets the drift specifications, at least for periods of weeks. A fallback solution uses a field programmable gate array to multiply the RHIC strobe by a selectable fraction. This system should be extremely stable, but has only a limited number of output frequencies.

The clock and trigger distribution board also interprets trigger words and distributes trigger information to the readout boards, and interprets and issue special triggers such as laser events and pulser signal triggers.

Many other elements of FEE were produced and installed in 1998. The list includes the power supplies, cabling, clock and trigger distribution cables. The slow controls systems and fiber readout bundles were procured, but not yet installed in 1998.

In cooperation with MPI, we designed and tested prototype FEE cards for the forward TPC[2]. The circuitry is similar to the main TPC design. However, the FTPC FEE cards each have 64 readout channels, squeezed into a board smaller than the 32 channel TPC FEE cards. Also, the shaping time is lengthened to 400 nsec and the tail correction controls will require re-optimization. Other minor modifications are required because the FEE card to readout board cables are considerably longer than with the main TPC.

References

[1] S. Klein *et al.*, "Front End Electronics for the STAR TPC," IEEE Transactions on Nuclear Science **43**, 1768 (1996).

[2] "The Forward Time Projection Chamber for the STAR Detector," F. Bieser *et al.*, MPI-PhE/98-3, Jan. 30, 1998.